MARKED-UP COPY OF AMENDED SPECIFICATION PARAGRAPHS:

Amend paragraph [0016] as follows:

[0016] FIG. ~~1D-2~~1E-2 shows a top view of FIG. 1D-1 in which several chips are back-bonded to a sacrificial layer and electrically connected thereto prior to the encapsulation step, according to the '671 disclosure.

Amend paragraph [0044] as follows:

[0044] In FIG. 1B, a plurality of pads 110 are selectively formed, typically by an electroplating operation, so that the pads 110 are disposed on and attached to the first surface 101 of the sacrificial layer 100. The pads 110 are arranged on the first surface 101 of the sacrificial layer 100 so as to define a central region 114 between the pads of a particular package group. The pads may be arranged in single rows around the central region 114 or may be arranged in multiple rows in a substantially grid array arrangement, an example of which is shown in FIG. 1D-2. The pads 100 in this embodiment are comprised of a first layer of copper 111 and a second layer of gold 112. Typically, there is also a center barrier layer (not shown) of nickel to ensure that the copper and gold layers do not diffuse into one another. The gold layer 112 facilitates a bond that is made by the electrical connection to the chip contacts, as described in more detail below. The height of the pads 110 is not critical so long as a good electrical connection can be made thereto. In some embodiments, the pads may resemble posts. Other examples of permissible pad materials include copper, nickel, gold, rhodium, platinum, silver and alloys and combinations thereof. Typically, in a low pin count package, the pads 110 are all of the same height from the sacrificial layer 100. However, for higher pin count packages or for other reasons, the pads 110 may not all be of the same height from the sacrificial layer 100. Taller pads 110 can be used in outside

rows of pads to ensure that the electrical connections between the contacts and the inner pads do not electrically short with the connections between the contacts and the outer pads. This can be useful in cases where the chip contacts are finely spaced or where the contacts are arranged in an area array on the face surface 121 of the chip 100, an example of which is shown in FIG. ~~1D-3~~1D-2.

Amend paragraph [0046] as follows:

[0046] Next, the chip contacts (not shown) on the face surface 121 of the chip 120 are each electrically connected to a respective pad 110 by wirebonding the one to the other, as shown in FIG. 1D-1. The wirebonded connection 130 could take the form of a ball bond/stitch (or wedge) bond combination, as shown, or the wire could be stitch-bonded to both the chip contacts and the pads 110. Other conventions could be used to interconnect the chip contacts and the pads, such as TAB leads, electroformed beam leads, etc. FIG. ~~1D-2~~1E-2 shows a top view of FIG. 1D-1.

Amend paragraph [0047] as follows:

[0047] The assembly, including the first surface 101 of the sacrificial layer 100, the pads 110, the chip 120 and the electrical connections, is next encapsulated (or over-molded) by a flowable, curable dielectric material 140, as by convention semiconductor molding technology, as shown in FIG. 1E. The dielectric material is typically comprised of filled or unfilled standard thermoset or thermo plastic resins as used in the industry, such as epoxy resin, silicone resin or other plastic encapsulating material. The dielectric material is then fully cured.

Amend paragraph [0049] as follows:

[0049] In FIG. 1G-1, the individual packaged chips 150 are "diced" or separated from each other. At this point, the

exposed bottom surfaces 113 of the pads 110 may be attached to respective bond pads on the PWB. One method of making such an attachment is to connect solder balls ~~160~~ to the bottom surface 113 of the pads 110. The solder balls ~~160~~ are typically comprised of a combination of tin and lead and may further coat a solid metal ball such that the solder balls ~~160~~ are non-collapsing. FIG. 1G-2 shows a bottom view of a multichip module embodiment of the '671 disclosure in which the packages are diced so that more than one chip 120 is included in the resulting package. FIG. 1G-2 could also be the top view of the undiced packages, as shown in FIG. 1F. While the above process is shown and described in an embodiment that packages more than one chip simultaneously, the process could also be used to package an individual chip if desired.

Amend paragraph [0050] as follows:

[0050] In an alternative method of manufacture shown in FIGS. 2A-E, the sacrificial layer is comprised of a dielectric polymer sheet 100' having a conductive layer 101', typically a thin layer of copper, on one surface of the sacrificial layer 100', as shown in FIG. 2A. An array of conductive pads 110' are next photo-lithographically defined by etching away undesired sections of the conductive layer 101' so that the pads 110' define a central region 114' therebetween. Within the central region 114', a central conductive region 115' may also be defined by the pad-forming lithographic process, as shown in FIG. 2B. A back surface 122' of a semiconductor chip 120' is then bonded to the conductive region 115' through the use of the thermally conductive die attach adhesive 135', as discussed in reference to FIG. 1. The chip contacts (not shown) on the exposed face surface 121' of the chip 120' are then electrically connected to respective pads 110' by wirebonding wires 130' therebetween. As discussed above, the elements are next

encapsulated in FIG. 2D using a suitable liquid encapsulant for the application and the encapsulant 140' is cured. Portions of the polymer sheet 100' are then removed, as by chemically etching or laser ablation operations, so that the pads 110' and central conductive region 115' are exposed. The packages may then be diced into either individual packages or multichip packages and connected to a PWB with conventional solder. Typically, the central region 115' is connected to the PWB in such a way that heat is drawn away from the chip into the PWB during operation of the package. As shown in the top plan view of FIG. 2F, a multichip package may include chips of different sizes that perform different functions. The addition of a dielectric, polymer sheet 100' allows this multichip module to have conductive paths 118' interconnecting at least some of the pads 110' within the multichip module thereby allowing signals to be transferred between the chips. It should be noted that if a wiring layer, such as is described in this multichip embodiment, is not needed or desired, the entire polymer sheet 100' may simply be removed by chemically dissolving the sheet leaving the pads and the central conductive region exposed.

Amend paragraph [0051] as follows:

[0051] FIG. 3 shows a still further embodiment of a packaged chip, similar to the packaged chips shown in FIG. 1G-1. In FIG. 3, however, a conductive protrusion ~~116''~~ 116' is electrically connected to a respective pad ~~110''~~ 110' and extends to the top surface ~~155''~~ 155' of the finished package ~~150''~~ 150' so that a top surface ~~117''~~ 117' of the protrusion ~~116''~~ 116' is exposed. This arrangement allows the bottom surface 113' of the pads 110' to be soldered to a supporting substrate (such as a PWB) while allowing another electronic component and/or semiconductor chip to be electrically connected to the packaged chip ~~150''~~ via the exposed top surface ~~117''~~

117' of the protrusions ~~116''~~116'; thus, creating a chip stacking technique. The protrusions may extend from every pad; however, typically they will extend from less than all of the pads.

Amend paragraph [0052] as follows:

[0052] In a further embodiment, FIG. 4A shows a side view of a microelectronic component ~~170'''~~170'' which is attached to the chip ~~120'''~~120''. The contacts on such a microelectronic component may be electrically connected between respective contacts on the chip ~~120'''~~120'' and/or may be connected to respective pads ~~110'''~~110''. Where the microelectronic component is a second semiconductor chip 170''', as shown in FIG. 4B, the back surface of the second chip ~~170''''~~170''' will be back-bonded to the face surface of the first chip ~~120''''~~ 120''' and the contacts on the second chip may be electrically connected to the contacts on the first chip ~~120''''~~120''' and/or to respective pads ~~110''''~~110'''. The pads ~~110''''~~ 110''' themselves may also be electrically interconnected.

Amend paragraph [0054] as follows:

[0054] Conductive pads 210 are next plated into the cavities 203 and apertures 205 so as to create the rivet-like pads 210, as shown in FIG. 5C. These pads 210 have a bottom bump flange 213 adjacent to the sacrificial layer 200 and integrally attached to a post pad 211 such that the post pad protrudes from the bump flange 213. A second bump flange 212 is integrally attached to the opposite end of the post pad 211. Both bump flanges 212/213 have flange areas that extend beyond the diameter of the post pad 211. FIGS. 5I-5J show alternate cross-sectional pad configurations, according to the present invention. In the embodiment shown in FIG. 5I, the pad is comprised of the bottom bump flange 213' and the post pad 211',

depicted in conjunction with sacrificial layer 200'. In FIG. 5J, the bump flanges 212'' and 213'', shown in conjunction with post pad 211'' and sacrificial layer 200'', are more squared off at the edges when compared to the rounded/oval bump flanges shown in the other FIGS. Other shape bump flanges may also be used.

Amend paragraph [0055] as follows:

[0055] In FIG. 5D, the photo-imageable layer 204 is removed leaving the pads 210 such that the pads within a particular group define a central region therebetween. A chip 220 is next back-bonded to the first surface of the sacrificial layer 200 using a thermally conductive die attach adhesive 235, as described in the previous embodiment. FIG. 5E shows electrical connections 230 interconnecting the chip contacts (not shown) on the face surface 221 of the chip 220 and the pads 210. The electrical connections 230 are made by using a wirebonder to stitch bond both ends of the wire to the pad 210 and the chip contacts. The stitch bonds create a low profile electrical connection between the contacts and the pads that, in turn, allows the finished package to be thinner. The pads 210, chip 220, and wires 230 are then encapsulated using an encapsulant 240, as described above in reference to FIG. 1 and further shown in FIG. 5F. The sacrificial layer is next etched away to expose the bottom bump flange 213, as shown in FIG. 2G. The packaged chips are then diced into either individual packaged chips or packaged multichip modules, as shown in FIG. 5H.

Amend paragraph [0056] as follows:

[0056] In a still further embodiment, FIGS. 6A-6F show another stackable chip arrangement. FIG. 6A-1 shows a side view in which a dielectric base material layer 305 is disposed on a top surface 302 of a sacrificial layer 300. The base material 305 is preferably comprised of a dielectric sheet-like layer,

such as polyimide. Typically, the base material 305 is laminated onto the sacrificial layer 300. Conductive pads 310 are disposed on the base material 305. The pads 310 may be plated on the base material 305 prior or subsequent to the base material's attachment to the sacrificial layer 300. FIG. 6A-2 shows a top plan view of FIG. 6A-1. The pads 310 in FIG. 6A-2 have bonding sites 315 and via sites 316. The pads 310 further define a central cavity 314. As shown in FIG. 6B-1, a semiconductor chip 320 is then back-bonded to the first surface 302 of the sacrificial layer 300 within the central cavity. The chip contacts (not shown) are next electrically connected to respective bonding sites 315 on the pads 310. Typically, the contacts are ~~wire-bonded~~connected to the respective bonding sites 315 by wire bonds 330. FIG. 6B-2 shows a top plan view of FIG. 6B-1.

Amend paragraph [0080] as follows:

[0080] After formation of the shells 906 the apertured layer 903 is removed from the first surface of the sacrificial layer 900, as shown in FIG. 9E. Next, as shown in FIG. 9F, a layer 907 of resistive material is deposited, using any of the methods previously described, over the first surface 901 of the sacrificial layer 900 such that the resistive layer 907 covers the first surface 901 of the sacrificial layer 900 and fills the interior spaces 911 of the shells. Thus, each shell or pad 906 and the resistive material 908 (Fig. 9G) within the shell forms a projection extending from the bottom surface of the resistive layer.

Amend paragraph [0093] as follows:

[0093] In an alternative embodiment, as shown in FIG. 12, a non-conductive apertured layer 1210, which is thicker than the patternable layer used in the embodiments shown in FIGS. 8A-8I, is applied across the first surface of the sacrificial layer~~,~~

~~and pads~~. Pads 1230 and posts 1240 are formed as discussed above with reference to FIGS. 8A-8I, so that the top bump flanges 1231 are initially in contact with the surface of the apertured layer. The apertured layer 1210 is etched or dissolved from the first surface of a sacrificial layer (not shown). However, the etching or dissolving process is arrested before the entire apertured layer 1210 has been removed. and a portion of layer 1210 remains on the first surface of the sacrificial layer. For example, if the apertured layer 1210 is comprised of a polymide, a hot caustic solution can be used to remove a portion of the patternable layer 1210. An etch rate may be selected for the hot caustic solution such that only a portion of the patternable layer is removed.

Amend paragraph [0097] as follows:

[0097] As shown in FIG. 14, a resistive device 1400 according to a further embodiment of the invention includes pads 1402, resistive layer 1403 and a heat sink 1404 overlying the top surface of the resistive layer, remote from the pads 1402. The heat sink 1404 is formed from a thermally-conductive material such as, for example, aluminum. Where the material of the heat sink is electrically conductive, a thin dielectric layer 1408 is provided between the base surface 1406 of the heat sink 1404 and the resistive layer 1403. For example, the base surface 1406 of the heat sink may be treated with an insulating finish such as epoxy or anodized. Alternatively, a dielectric layer may be provided on the resistive layer as, for example, by a molding process as discussed above with reference to Figs. 11A-11E, or by laminating the dielectric layer to the resistive layer. In a further variant, the heat sink and dielectric may be provided as a unit which is applied in place of a simple dielectric layer in a molding process as described with reference to Figs. 11A-11E. The heat sink 1404 allows the resistive device 1400 to dissipate

more power without overheating. While the resistive device 1400 as shown in FIG. 14 is manufactured by the method as shown in FIGS. 9A-9H, resistive devices manufactured by any other method of manufacturing resistors described herein may be mounted onto a heat sink in similar fashion.

MARKED-UP COPY OF AMENDED CLAIMS:

1. A method of making at least one resistor, the method comprising:

providing a sacrificial layer having a first surface and one or more pads including at least one electrically conductive material disposed over at least one region of said first surface;

depositing ~~a~~ an electrically resistive material over said pads and over said first surface of said sacrificial layer to thereby form at least one unit including said electrically resistive material and said one or more pads;

removing at least a portion of said sacrificial layer to expose said one or more pads. to form said at least one resistor.

2. The method as claimed in claim 1, wherein a plurality of resistors is manufactured simultaneously using a single sacrificial layer, the method further comprising separating at least some of said resistors from one another after at least a portion of the sacrificial layer has been removed.

6. The method as claimed in claim 5 wherein said step of providing said cavities in said first surface includes providing an apertured layer on said first surface and etching said first surface through ~~the~~ apertures in said apertured layer.

10. The method as claimed in claim ~~5~~6, further comprising removing at least a portion of said apertured layer from said first surface of said sacrificial layer.

18. The method as claimed in claim 16 wherein said step of depositing said electrically resistive material is performed so as to embed one flange and at least a part of the post of each said pad in the electrically resistive material while leaving at least part of the other flange of each said pad exposed at a surface of said electrically resistive material.

22. The method as claimed in claim 1, further comprising removing excess electrically resistive material from each said unit using a bulk trimming process.

23. The method as claimed in claim 1, further comprising providing a heat sink having a first surface wherein said electrically resistive material forms ~~a~~ an electrically resistive layer having a first surface and a second surface, wherein said first surface of said electrically resistive layer is connected to said first surface of said heat sink.

24. The method as claimed in claim 1, further comprising before depositing said electrically resistive material, providing an insulating layer having a first surface and a second surface, wherein said electrically resistive material is deposited between said second surface of said insulating layer and said first surface of said sacrificial layer.

25. The method as claimed in claim 24, wherein a plurality of resistors are manufactured simultaneously using a single sacrificial layer and a common insulating layer, the method further comprising separating at least some of said resistors from one another after removing at least a portion of the sacrificial layer, wherein said separated resistors remain connected to said common insulating layer.

26. The method as claimed in claim 1, further comprising trimming said electrically resistive material in at least one said unit to control ~~the resistive value~~electrical resistance of ~~said resistive material~~at least one said unit.

29. A method of making at least one resistor, the method comprising:

providing a sacrificial layer having a first surface and a plurality of cavities in the first surface of said sacrificial layer;

depositing one or more conductive materials within said cavities to form conductive pads within said cavities—;

disposing an electrically resistive material over the first surface of the sacrificial layer and the pads to thereby form one or more units; and

removing at least a portion of said sacrificial layer to expose said pads.

30. The method of claim 29 wherein said step of depositing one or more conductive materials is performed so as to form said pads as hollow shells within said cavities, and wherein said step of disposing electrically resistive material includes applying said electrically resistive material into said hollow shells.

31. The method as claimed in claim 29, wherein a plurality of resistors are manufactured simultaneously using the same sacrificial layer, the method further comprising a step of separating at least some of the resistors from one another after at least a portion of the sacrificial layer has been removed.

35. The method as claimed in claim 33, further comprising removing at least a portion of said apertured layer from said first surface of the sacrificial layer before depositing said electrically resistive material.

36. The method as claimed in claim 35, wherein all of said patternable layer is removed from the first surface of the sacrificial layer before depositing said electrically resistive material.

37. The method as claimed in claim 29, further comprising, before depositing said electrically resistive material, providing an insulating layer having a first surface and a second surface, wherein said resistive material is deposited between said second surface of said insulating layer and said first surface of said sacrificial layer.

38. A method of making at least one resistor, the method comprising: including an electrically conductive material

providing a sacrificial layer having a first surface and a second surface;

depositing an electrically resistive material over said first surface of said sacrificial layer so that said resistive material adheres to said sacrificial layer; and

selectively removing portions of said sacrificial layer to form one or more pads connected to said resistive material.

39. A method as claimed in claim 38 wherein said first surface of said sacrificial layer is rough, and the roughness of said first surface promotes adhesion between said sacrificial layer and said electrically resistive material.

42. The method as claimed in claim 38, further comprising before depositing said electrically resistive material, providing an insulating layer having a first surface and a second surface, wherein said resistive material is deposited between said second surface of said insulating layer and said first surface of said sacrificial layer.

REMARKS

The present Amendment is presented in response to the Official Action mailed December 14, 2001. A Petition for a two-month extension of the term for response to said Official Action, to and including May 14, 2002, is transmitted herewith.

The objection to the drawings is noted. The specification has been amended to conform the reference numerals used in the specification with the reference numerals used in the drawings. Also, the drawings have been amended to correct the duplicate figure number noted in the draftperson's patent drawing review (Form PTO 948). The specification has been amended where appropriate to refer to the corrected figure number.

In a telephone conversation between undersigned counsel and Examiner Chambliss on May 13, 2002, it was indicated that the substitute specification filed on or about May 21, 2001 has been entered and, accordingly, the present amendments are made with reference to that specification.

The drawings have been further amended to delete two extraneous reference numerals from FIG. 15. Red-marked prints of the drawings showing the changes are transmitted herewith, along with corrected formal pages. Reconsideration of the drawing objection is respectfully requested in light of the amended specification and drawings.

The abstract has been cancelled and replaced by a new abstract.

Claims 1-42 were rejected under 35 U.S.C. § 112, second paragraph as assertedly indefinite. The claims have been amended in response to this rejection. Before addressing some of the specific points raised in this rejection, it is believed worthwhile to summarize the way in which certain embodiments disclosed in the specification operate. Merely by way of example, in the embodiment of FIG. 9, a sacrificial layer 900 is

provided with pads 906 on a first surface (the upwardly-facing surface in FIG. 9E). A layer 907 of an electrically resistive material is deposited on the first surface of the sacrificial layer and, hence, on the pads 906. The electrically resistive material is a material which will conduct electricity but which has substantial resistance as, for example, a mixture of metallic or carbon particles and a binder. (Specification, ¶ 70.) That mass of electrically resistive material and pads forms one or more resistors. Thus, when the sacrificial layer 900 is removed, the pads 906 are exposed. The resulting product has the desired electrical resistance between pads 906; the electrically resistive material provides a conductive path with the desired resistance. As seen, for example, in Figs. 9E-9H, multiple resistors or "units" can be made by applying a single layer of resistive material 907 on the same sacrificial layer 900 and then severing the layer so as to separate two or more units from one another (FIG. 9H).

Turning to the specifics of the § 112, second paragraph rejections, the phrase "resistive material" has now been clarified to recite -- electrically resistive material --. That phrase was used in the application as filed as, for example, in originally-filed claim 43 (now withdrawn from consideration).

As to claims 2, 25 and 35, applicant is not implying that the sacrificial layer and pads form a resistor; the resistor is formed by the pads and the deposited "electrically resistive material." As explained above, the electrically resistive material is deposited on a single sacrificial layer. The recitation that plural resistors are formed simultaneously "using a single sacrificial layer" is believed to be clear in this context. In response to the rejection of claim 2, however, the phrase "separating at least some of said resistors" has been clarified to more clearly point the step of "separating at least

some of said resistors from one another." Claim 6 has been modified to delete the phrase "the apertures" and simply refer to "apertures." Antecedent basis for the phrase "said apertured layer" in claim 10 has been provided by amending claim 10 to depend from claim 6, which recites the apertured layer.

Claim 18 now refers to "each said pad." As claim 18 depends from claim 16, which in turn depends from claim 1, and as claim 1 recites positively the step of providing "pads," antecedent basis has been provided.

As to claim 20, the recitation that the sacrificial layer "includes a dielectric defining said first surface" is not unclear; it is generic. It embraces both an embodiment in which the dielectric material constitutes the entire sacrificial layer and an embodiment in which the dielectric layer is provided only at the first surface of the sacrificial layer. Also, because claim 20 recites the step of "disposing a seed layer on said first surface of said sacrificial layer" and because the claim says that the dielectric "defines said first surface" of the sacrificial layer, the dielectric and the seed layer cannot be "one and the same."

As to claim 25, the location of the insulating layer relative to the sacrificial layer and the electrically resistive material is believed to be clear in context of claim 24, from which claim 25 depends. Claim 24 says positively that the electrically resistive material is deposited "between said second surface of said insulating layer and said first surface of said sacrificial layer." An example of this arrangement is shown in Figs. 11A-11E. The electrically resistive material 1140 is deposited between the sacrificial layer 1100 and the common insulating layer 1120.

Claim 26 has been modified to state that the step of trimming the resistive material is performed to control "electrical resistance of at least one said unit." In the

context of an electrical resistor, "trimming" or removing some of the resistive material does not alter the volume resistivity of the material, but instead alters the cross-sectional area of the conductive pathway through the material.

Claim 40 is also believed to be clear in context of claim 38 and in context of the specification and drawings (*e.g.*, Figs. 10A-10G). In the process recited in claim 38 and incorporated in claim 40 by dependency, the pads are not provided on the first surface of the sacrificial layer as discussed above with reference to claim 1. Instead, the pads are formed from the sacrificial layer itself. For example, in FIG. 10F, an electrically resistive material 1003 is provided on a sacrificial layer 1000 and etch resistant material 1006 is provided on the opposite side of the sacrificial layer. Etching the sacrificial layer leaves portions of the sacrificial layer 1007 forming the pads. It is respectfully submitted that the claims as now amended are clear and definite in accordance with § 112, second paragraph.

Claim 1 was rejected under 35 U.S.C. § 102(b) as supposedly anticipated by *Tanaka*, JP 03-0094459A. Reconsideration and withdrawal of this rejection are respectfully requested. *Tanaka* '459 makes a chip package and does not make a "resistor" as recited in claim 1. In this context, applicant uses the term "resistor" in accordance with its well-understood meaning in the electrical and electronic arts, namely, "a device used to control current in an electric circuit by providing resistance." *American Heritage Dictionary Of The English Language*.

In this context, the term "electrically resistive material" as used in claim 1 refers to a material which conducts electricity with a desired resistance, and which provides the resistance in the completed electrical resistor. As noted above, some of the preferred electrically resistive materials

used in the process of claim 1 are conductive or semiconductive materials such as metal or carbon particles in a binder having controlled resistivity set by the composition of the material as, for example, the proportions of conductive particles used. (*See* ¶ 70 of the specification.) By contrast, the material 22 applied in *Tanaka* '459 is a "sealing resin 22" used to encapsulate a wire-bonded semiconductor chip. The Official Action manifestly does not point out anything in the reference which suggests that this material could serve as an electrically resistive material in a resistor, as required by claim 1. Indeed, it is believed clear from the reference itself that sealing material 22 must be a dielectric, *i.e.*, a material which for all practical purposes does not conduct electricity at all. If it were not, the various connections to the semiconductor chip would be connected in common ("shorted") with one another, rendering the chip useless. As *Tanaka* '459 does not make a resistor and does not apply an "electrically resistive material" as referred to in claim 1, *Tanaka* '459 does not anticipate claim 1, and the rejection should be withdrawn with respect to claim 1 and with respect to claims 4, 5, 10-12, 14, 15, 20, 24 and 27, dependent thereon. The same reasons apply with respect to claim 29. Here again, *Tanaka* '459 does not make "at least one resistor" and does not dispose an "electrically resistive material" over the surface of the sacrificial layer and the pads, as recited in claim 29. The same reasons apply with regard to claim 37. As to claim 38, *Tanaka* '459, again, does not make a resistor and does not deposit an electrically resistive material on a surface of a sacrificial layer.

Claims 2, 3, 25, 26 and 31 were rejected under 35 U.S.C. § 103 on *Tanaka* '459 as applied to claim 1 "further in view of *Lake et al.*, U.S. Patent 5,937,512." This rejection should be withdrawn for substantially the same reasons as discussed above in connection with the § 102 rejection on *Tanaka*

'459 alone. *Lake* '512 has not been cited as teaching anything which would remedy the deficiencies of *Tanaka* '459 discussed above.

The Examiner's indication that certain claims would be allowable if rewritten to overcome the § 112 rejections, and if rewritten in independent form, is noted with appreciation. However, these claims have not been rewritten into independent form at the present time, as it is believed that the independent claims are allowable for the reasons set forth above.

As it is believed that all of the objections, rejections and requirements set forth in the Official Action have been fully met by the foregoing amendments and remarks, favorable reconsideration and allowance of all claims in the application are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: May 14, 2002

Respectfully submitted,

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